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CLAIMS

1   1.   A method for establishing timing synchronism between a transmitter
2   symbol clock and a local symbol clock in a receiver for receiving a signal transmitted
3   as a sequence of symbols at a symbol frequency and subject to exhibiting a symbol
4   frequency offset, said method comprising the steps of:
5   calculating a preselected number of offset values for a desired symbol timing
6   recovery range, said offset values being grouped substantially symmetrically about a
7   central offset value;
8   testing each of said preselected offset values to see if symbol timing recovery
9   lock can be achieved by starting at said central offset value and gradually moving
10   away from said central offset value.

1   2.   A method of claim 1 wherein the received signal carries a high
2   definition television (HDTV) signal transmitted as a modulated vestigial sideband
3   (VSB) signal formatted as a one-dimensional data constellation of symbols
4   representing digital image data.

1   3.   A method as claimed in claim 1 wherein said desired symbol timing
2   recovery range is plus or minus 1 kHz.

1   4.   A method as claimed in claim 3 wherein said preselected number of
2   offset values is nine.

1   5.   A method as claimed in claim 4 wherein said nine offset values are 0
2   Hz; plus or minus 200 Hz; plus or minus 400 Hz; plus or minus 600 Hz; and plus or
3   minus 800 Hz.

1   6.   A method as claimed in claim 1 further comprising steps of repeating
2   the testing step for each of a plurality of symbol timing recovery algorithms.

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1   7.   A method as claimed in claim 6 wherein said plurality of symbol timing
2   recovery algorithms comprises the Mueller and Muller algorithm and the Gardner
3   algorithm.

1   8.   A processor for establishing timing synchronism between a transmitter
2   symbol clock and a local receiver symbol clock in a receiver for receiving a signal
3   comprising a sequence of symbols at a symbol frequency and subject to exhibiting
4   symbol frequency offset comprising:
5   means for calculating a preselected number of offset values for a desired
6   symbol timing recovery range, said offset values being grouped substantially
7   symmetrically about a central offset value;
8   means for testing each of said preselected offset values to see if symbol
9   timing recovery lock can be achieved by starting at said central offset value and
10 gradually moving away from said central offset value.

1   9.   A processor as claimed in claim 8 wherein the received signal
2   comprises a high definition television (HDTV) signal transmitted as a one-
3   dimensional data constellation of symbols representing digital image data.

1   10.   A processor as claimed in claim 8 wherein said desired symbol timing
2   recovery range is plus or minus 1 KHz.

1   11.   A processor as claimed in claim 10 wherein said preselected number of
2   offset values is nine.

1   12.   A processor as claimed in claim 11 wherein said nine offset values are
2   0 Hz; plus or minus 200 Hz; plus or minus 400 Hz; plus or minus 600 Hz; and plus
3   or minus 800 Hz.

1   13.   A processor as claimed in claim 12 further comprising:
2   means for using a plurality of symbol timing detection algorithms for said
3   testing; and

4   means for switching between said algorithms as desired to maximize the
5   possibility of STR lock.

1   14.   A processor as claimed in claim 13 wherein the switching means
2   comprises means for selecting one of the plurality of detection algorithms before
3   testing each of said preselected offset values.

1   15.   A processor as claimed in claim 13 wherein said plurality of timing
2   detection algorithms comprise the Mueller and Muller algorithm and the Gardner
3   algorithm.